PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing
(day/month/year) see form PCT/ISA/210 (second sheet)

Applicant's or agent's file reference
see form PCT/ISA/220

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/JP2004/019291	16.12.2004	18.12.2003

International Patent Classification (IPC) or both national classification and IPC
G11C13/00

Applicant
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☒ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

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Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material:

   ☐ in written format

   ☐ in computer readable form

   c. time of filing/furnishing:

   ☐ contained in the international application as filed.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

Box No. IV Lack of unity of invention

1. ☐ In response to the invitation (Form PCT/ISA/206) to pay additional fees, the applicant has:

   ☐ paid additional fees.

   ☐ paid additional fees under protest.

   ☐ not paid additional fees.

2. ☒ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.

3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is

   ☐ complied with

   ☒ not complied with for the following reasons:

   see separate sheet

4. Consequently, this report has been established in respect of the following parts of the international application:

   ☒ all parts.

   ☐ the parts relating to claims Nos.

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	9-11
	No:	Claims	1-8
Inventive step (IS)	Yes:	Claims	10
	No:	Claims	9,11
Industrial applicability (IA)	Yes:	Claims	1-11
	No:	Claims	

2. Citations and explanations

   see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Reference is made to the following documents:

D1: US-6-204-139

D2: US-6-473-332

D3 : "Electric-pulse-induced reversible resistance change effect in magnetoresistive films", Liu S Q; Wu N J; Ignatiev A, APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS, NEW YORK, US XP012025238

D4 : US-2003-0003674

Re Item IV

Lack of unity of invention

Independent claims 1 and 9 relate to a method of initializing a variable-resistance. Independent claim 5 relates to a variable-resistance connected to a fixed resistor used during read. The only common concept is the variable-resistance, which is known from the prior art. Hence, the Application does not relate to one single group of inventions linked by a single general inventive concept as required by Rule 13 PCT.

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

For the further purposes of this report it will be assumed that the objections of paragraph **Item VIII** were overcome by appropriate amendment of the claims.

1.1 The subject-matter of **claim 1** is not new in the sense of Article 33(2) PCT. Document D1 discloses in its figure 4a or 4b a method for initializing a material (variable-resistance material $Gd_{0.7}Ca_{0.3}BaCo_2O_{5+5}$ or PCMO film) whose resistance value increases/decreases according to the polarity of an applied electric pulse (the first resistance value in the graphs before the application of any electric pulse is not the high or low resistance value used to store information, and this first value is changed and initialized to a low or high resistance value with application of electric pulses), wherein an electric pulse having a first polarity (-12V or 51V) is applied at least once between first and second electrodes connected to the variable-resistance material such that the potential of the first electrode is higher than that of the second electrode.

1.2 D1 discloses further the features of **claims 2, 3 and 4** :
-that the first electric pulse is repeatedly applied between the first and second electrodes (see the first four electrical pulses at -12V of fig.4a) till the variation rate of the resistance value of the variable-resistance material becomes smaller than a predetermined value (for the last three electrical pulses the variation is smaller than 10 ohms),
-that an electric pulse having a second polarity (see the following seven electrical pulses at +12V of fig.4a) is applied at least once between first and second electrodes connected to the variable-resistance material such that the potential of the first electrode is lower than that of the second electrode (opposite polarity) (the initialization is done with the -12V and +12V because if only the -12V are applied, the resistance obtained is higher than the maximal resistance obtained normally afterwards and thus the material is not yet initialized to his normal values),
-that the second electric pulse is repeatedly applied between the first and second electrodes (see following seven electrical pulses at +12V of fig.4a) till the variation rate of the resistance value of the variable-resistance material becomes smaller than a predetermined value (for the last two electrical pulses at +12V the variation is smaller than 25 ohms).

1.3 For the sake of completeness, it is added that D2 discloses also the steps of method **claim 1** since the variable-resistance material (110) whose resistance value increases/decreases according to the polarity of an applied electric pulse is put to an initial resistive state by applying a reset electric pulse (see col 4 lines 9-13).
It has to be mentioned that, in fact, any first programing is an initialization. Hence, D3 in its figure 1 discloses the steps of **claims 1 to 2.** As it is obvious to proceed afterwards to an erase (programming with opposite polarity), the steps of **claims 3 to 4** in view of D3 are not inventive.

2. 1 The subject-matter of **claim 5** is not new in the sense of Article 33(2) PCT.
Document D2 discloses in its fig.2, 5, 6 and 7 a memory device ((532) or (504), and (538)) formed using a material (variable-resistance material (208), PCMO or LSMO or GBCO) whose resistance value increases/decreases according to the polarity of an applied electric pulse, comprising:
-a variable-resistance material (208) to which first (212) and second (214) electrodes are

connected; and
-a fixed resistor (Rin (520)), one end of which is connected to the first or second electrode wherein an electric pulse is applied for recording between the first and second electrodes (see fig.6).

2.2 D2 discloses further that :
-memory information is read based on a voltage (VR) between the first and second electrodes which is obtained when a predetermined voltage (VS) is applied between one of the first and second electrodes which is not connected to the one end of the fixed resistor and the other end of the fixed resistor (see table of fig.7 with the values of VR),
-memory information is read based on a voltage (potential of input node of differential amplifier (502)) between the ends of the fixed resistor which is obtained when a predetermined voltage (Vs) is applied between one of the first and second electrodes which is not connected to the one end of the fixed resistor and the other end of the fixed resistor (see fig.5),
-the variable-resistance material (208) is initialized in advance by the initialization method recited in any one of claims 1 to 4 (the first write initializing the variable-resistance).
Hence, the features of **claims 6, 7 and 8** are known from D2.

3. D4 discloses in its figure 1 and 3 a memory circuit including first ((52) connected to W1 and B1) and second ((52) connected to W1 and B2) variable resistors connected in series between a first terminal (B1) and a second terminal (B2) wherein the first variable resistor being connected between the first terminal (B1) and a third terminal (W1) and having a resistance value which increases/decreases according to the polarity of a pulse voltage applied between the first terminal and the third terminal (see paragraph [0028]), and the second variable resistor being connected between the third terminal (W1) and the second terminal (B2) and having a resistance value which increases/decreases according to the polarity of a pulse voltage applied between the third terminal and the second terminal (see also paragraph [0028]).
D4 also discloses a block erase method wherein both cells are put at the same time to the same high or low resistance value (see paragraph [0025] and [0027]) : hence D4 discloses the steps of applying a first pulse voltage having a first polarity between the first terminal and the third terminal at least once and applying a second pulse voltage

having a second polarity between the third terminal and the second terminal at least once.

In D4 the two variable resistors are made of $Gd_{0.7}Ca_{0.3}BaCo_2O_{5+5}$ with bottom electrode made of YBCO or PCMO with bottom electrode made of platinum (see paragraphs [0014] and [0015]).

According to fig.4a or fig.4b of D1, when these variable resistors have not yet been subjected to application of a pulse voltage (electrical pulse number =0), they have an arbitrary initial resistance which corresponds neither to their high or low resistance state read afterwards during operation. D1 discloses that by applying a first pulse voltage and after an opposite pulse voltage, the variable resistors are initialized and afterwards achieve stable high or low resistance value.

Hence the person skilled in the art would be prompted to, in an initial state where the first and second resistors have not yet been subjected to application of a pulse voltage, perform a block erase, i.e apply a first pulse voltage having a first polarity between the first terminal and the third terminal at least once and applying a second pulse voltage having a second polarity between the third terminal and the second terminal at least once, and after this block erase, to apply a third pulse voltage having a polarity opposite to the pulse voltage applied just before to both variable resistors (at least one variable resistor would be programmed).

Hence, the steps of method **claims 9 and 11** are not inventive in view of D4 combined with the teaching of D1.

Re Item VIII

Certain observations on the international application

1. In claim 1, 5, the bracketed expression "(variable-resistance material)" which does not contain a reference sign is unclear (Art. 6 PCT). First, the bracket render unclear whether the feature introduced is limiting or not. Second, the expression "variable-resistance material" could refer only to a material having just a variable resistance or to the specific materials disclosed by D2 (see page 1 of the description).

2. In claim 1, the expression "a method for initializing" is unclear (Art. 6 PCT). An initial state can be any state defined as origin. However, according to the description, it is clear

that the first pulse voltage is applied in an initial state where the variable-resistance material have not yet been subjected to application of a pulse voltage.